

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-21 and 25-28 are pending in this application, Claims 1-3, 5, 7, 8, 16-20, and 25-27 having been currently amended. Support for amended Claims 1-3, 5, 7, 8, 16-20, and 25-27 can be found, for example, in the original claims, drawings, and specification as originally filed.¹ No new matter has been added.

In the outstanding Office Action, Claims 1-9, 17, 19-21, and 25-29 were rejected under 35 U.S.C. § 103(a) as unpatentable over Aweya et al. (U.S. Patent No. 7,043,651; hereinafter “Aweya”) in view of Zdepski (U.S. Patent No. 5,467,137); and Claims 10-16 and 18 were rejected under 35 U.S.C. § 103(a) as unpatentable over Aweya in view of Zdepski and Lahat (U.S. Patent No. 6,963,561).

In response to the rejection of Claims 1-9, 17, 19-21, and 25-29 under 35 U.S.C. § 103(a) as unpatentable over Aweya in view of Zdepski, Applicants respectfully submit that amended independent Claim 1 recites novel features clearly not taught or rendered obvious by the applied references.

Amended independent Claim 1 is directed to a method of synchronizing the phase of a local image frame synchronization signal generator including, *inter alia*:

...frequency synchronizing said local and reference clocks;

said reference video data processor sending, via said network, to said local data processor one image timing packet providing reference image frame synchronization data indicating a difference in timing, measured with respect to said reference processor's clock, between a time at which said image timing packet is launched onto said network and a time

¹ See page 4, line 33 to page 5, line 28; page 10, lines 6-23; page 11, lines 32-33; and page 12, lines 3-7 of the specification; and original Claim 7.

of production of a reference image frame synchronization signal;

said local video data processor controlling the phase of production of said local image frame synchronization signals in dependence on said reference image frame synchronization data and a time of arrival of said one image timing packet; and

sending to said local video data processor from said reference video data processor, via said network, data packets containing said video data, said image timing packet being sent independently of said data packets.

Independent Claims 25-27 recite substantially similar features as independent Claim

1. Therefore, the arguments presented below with respect to Claim 1 are also applicable to independent Claims 25-27.

Applicants respectfully submit that Aweya fails to teach or suggest that one image timing packet is sent independently of data packets containing video data, as recited in Applicants' amended independent Claim 1. In contrast, in Aweya, synchronization patterns are inserted periodically into the bitstream at the transmitter.² Furthermore, Aweya describes that each data packet carries a timestamp.³ Therefore, in Aweya, there is no description of timing packets which are sent independently of the data packets, because ***the timestamp is part of the data packet.***

Furthermore, Aweya does not teach or suggest the use of image frame synchronization data or frame synchronization signals, as recited in Applicants' Claim 1. In a non-limiting embodiment of Applicants' invention, a local frame sync signal and a reference frame sync signal are used to carry out frame synchronization at the destination.⁴ In particular, Applicants' claimed invention as recited in Claim 1 controls the phase of production of the local image ***frame*** synchronization signals in dependence upon the reference image ***frame*** synchronization data and a time of arrival of the one image timing

² See column 3, lines 23-24 of Aweya.

³ See column 12, lines 22-24 of Aweya.

⁴ See page 9, line 28 to page 11, line 30 of the specification.

packet. Therefore, from at least the passages on pages 9 to 11 of Applicants' specification, it is clear that the use of an *image frame* synchronization signal is different from synchronizing the local and reference clocks. In contrast, Aweya merely synchronizes clocks in a network rather than controlling the phase of local image frame synchronization signals.⁵ Therefore, Applicants respectfully submit that there is nothing in Aweya which teaches or suggests the use of frame synchronization signals and frame synchronization data, as recited in Claim 1.

Turning now to Zdepski, Zdepski describes that the *count values are embedded in the transport packets*.⁶ Therefore, although Zdepski describes the use of auxiliary transport packets,⁷ there is nothing in Zdepski which teaches or suggests that one image timing packet is sent independently of data packets containing video. Furthermore, Zdepski merely controls the receiver clock signal using the differences of successive sampled count values which are compared with differences of corresponding successive combined count values.⁸ Therefore, Zdepski merely relates to video synchronization rather than synchronized delivery over a network. In Zdepski, it is the *clock* which is synchronized,⁹ rather than the phase of local image frame synchronization signals as in the Applicants' independent claims. Therefore, nowhere does Zdepski teach or suggest controlling the *phase* of production of the local image frame synchronization signals.

Additionally, in response to point 2 in the Response to Arguments section of the outstanding Office Action, in which the "Examiner asserts that the measurement of time delay with reference to the original signal meets the definition of 'phase,'" it is noted that the Examiner is referring to the *measurement of phase*. Notwithstanding the differences between synchronizing a clock and the frame synchronization signals as mentioned above,

⁵ See column 4, lines 54-55 and column 7, lines 52-55 of Aweya.

⁶ See column 2, lines 3-10 of Zdepski.

⁷ See Figure 7, and column. 5, lines 49-67 of Zdepski.

⁸ See column 2, lines 23-27 of Zdepski.

⁹ See column 5, lines 3-28 of Zdepski.

Zdepski does not teach or suggest controlling the phase of production of synchronization signals. Zdepski synchronizes the *frequency* (i.e. controls the frequency). However, even if the Examiner's interpretation of phase is assumed to be correct, at most Zdepski describes synchronizing the frequency of the clocks based on the *measurement* of a phase difference. This is entirely different from controlling the phase as in Applicants' amended Claim 1.

Neither Aweya nor Zdepski teach or suggest the use of image *frame* synchronization signals and image *frame* synchronization data, as in Applicants' Claim 1. Both Aweya and Zdepski merely relate to the synchronization of clocks, whereas, in the claimed invention, the synchronization of the local and reference clocks is different from controlling the phase of production of the local image frame synchronization signals in dependence upon the reference image frame synchronization data and a time of arrival of the one image timing packet.

Furthermore, neither Aweya nor Zdepski teach or suggest that the image timing packet is sent independently of data packets containing video data. Therefore, a person ordinarily skilled in the art could not arrive at Applicants' Claim 1 by combining the teachings of Aweya with Zdepski. Additionally, there is no motivation for a person of ordinary skill in the art to combine Aweya with Zdepski. In Aweya, the timestamp is part of the data packet, thus rendering the system of Aweya incompatible with the auxiliary transport packets of Zdepski.

By using frame synchronization signals and frame synchronization data as recited in the amended independent claims, the claimed invention advantageously allows a separate frame sync counter to be controlled independently from a clock sync counter. For example, the frame sync counter can be reset to a different time to the clock sync counter, thus allowing the use of multiple frame rates without affecting the synchronization of the clocks.

Furthermore, because the image timing packet is sent independently from the data packets, the image timing packet can have the highest switch priority. This means that the amount of jitter introduced into the network can be minimized and the clock synchronization can be as precise as possible. Additionally, the use of just one image timing packet minimizes delay and jitter because the one image timing packet does not have to contend with other image timing packets. These advantages, together with the novel features as mentioned above which provide these advantages, are neither taught nor suggested by Aweya or Zdepski, either alone or in proper combination.

Thus, Applicants respectfully submit that independent Claims 1 and 25-27 (and all claims depending thereon) patentably distinguish over Aweya and Zdepski.

Accordingly, Applicants respectfully request that the rejection of Claims 1-9, 17, 19-21, and 25-29 under 35 U.S.C. § 103(a) as unpatentable over Aweya in view of Zdepski be withdrawn.


In response to the rejection of Claims 10-16 and 18 under 35 U.S.C. § 103(a) as unpatentable over Aweya in view of Zdepski and Lahat, Applicants note that Claims 10-16 and 18 are dependent on Claim 1, and are thus believed to be patentable for at least the reasons discussed above. Further, Applicants respectfully submit that Lahat fails to cure any of the above-noted deficiencies of Aweya and Zdepski.

Accordingly, Applicants respectfully request that the rejection of Claims 10-16 and 18 under 35 U.S.C. § 103(a) as unpatentable over Aweya in view of Zdepski and Lahat be withdrawn.

Consequently, in view of the present amendment, and in light of the above discussion, the pending claims as presented herewith are believed to be in condition for formal allowance, and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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